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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/848,642	05/03/2001	Shunpei Yamazaki	SEL 258	7227
7590 COOK, ALEX, MCFARRON, MANZO, CUMMINGS & MEHLER, LTD. Suite 2850 200 West Adams St. Chicago, IL 60606			EXAMINER SCHECHTER, ANDREW M	
			ART UNIT 2871	PAPER NUMBER
			MAIL DATE 08/06/2008	DELIVERY MODE PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/848,642	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	ANDREW SCHECHTER	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 02 July 2008.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 21-24, 76, 77 and 85-102 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) 21-24, 76, 77, 85-90, 93, 94, 97 and 98 is/are allowed.
 6) Claim(s) 91, 92, 95, 96, 99 and 100 is/are rejected.
 7) Claim(s) 101 and 102 is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 05 March 2004 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ . |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>7/2/08</u> . | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| | 6) <input type="checkbox"/> Other: _____ . |

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 2 July 2008 has been entered.

Response to Arguments

2. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

In view of the terminal disclaimers filed on 2 July 2008, the previous double patenting rejections are withdrawn.

The amendments to independent claims 91 and 92 have broadened the scope of these claims; the following rejections are now appropriate.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 91, 92, 95, 96, 99, and 100 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Sakamoto*, Japanese Patent Document No. 9-160509 (made of record with a translation by the applicant) in view of *Yokomizu*, Japanese Patent Document No. 10-073813, *Nagayama et al.*, U.S. Patent No. 5,680,187, *Kanemoto et al.*, U.S. Patent No. 5,493,429, and *Yoneya et al.*, U.S. Patent No. 6,300,926.

Sakamoto discloses [see Fig. 2, for instance] an electro-optical device comprising a first substrate [20], a TFT formed over the first substrate comprising a gate electrode [1], a first insulating film [4] formed on said gate electrode, a semiconductor layer [5] formed over the first insulating film, and having at least a source region [6], a drain region [7], and a channel formation region [between them; note that the labels ‘source’ and ‘drain’ are reversed in the reference, though the structure is the same]; a source wiring [2] formed over the first substrate, the source wiring electrically connected to the source region [via 12], wherein the first insulating film is formed on the source wiring; a second insulating film [11] over the semiconductor layer, a pixel electrode [15] comprising a first transparent conductive film [ITO, see paragraph 0017], and electrically connected to the drain region [via 13], and a liquid crystal [see paragraph 0001].

Sakamoto does not necessarily explicitly disclose (at least for this embodiment) a second substrate opposed to the first substrate, at least a first colored layer and a second colored layer formed in the second substrate, partly overlapping each other; an organic resin film covering the first and second colored layer; an opposing electrode comprising a second transparent conductive film; a liquid crystal interposed between the

pixel electrode and opposing electrode, wherein the organic resin film is interposed between the liquid crystal and the first and second colored layers and has a thickness of 1 μm or more, and the opposing electrode is interposed between the liquid crystal and the organic resin film.

Yokomizu discloses [see Figs. 1 and 2, for instance] an analogous electro-optical device comprising a first substrate [10], a thin film transistor [paragraph 0017] formed over the first substrate, a pixel electrode [13] comprising a first transparent conductive film [paragraph 0018], and electrically connected to the TFT, a second substrate [20] opposed to the first substrate, at least a first colored layer [21B] and a second colored layer [21R] formed on the second substrate wherein the first and second colored layers partly overlap each other to form a light shielding portion [21BM]; an organic resin film [22, paragraph 0021] covering said first and second colored layers and said light shielding portion, an opposing electrode [23] comprising a second transparent conductive film [paragraph 0021], and a liquid crystal [30] interposed between the pixel electrode and the opposing electrode, wherein the organic resin film is interposed between the liquid crystal and the first and second colored layers, and wherein the opposing electrode is interposed between the liquid crystal and the organic resin film.

(The examiner notes that the limitation relating to the overlap of a light shielding portion and the channel formation region has been deleted from claims 91 and 92 and amended to claims 101 and 102, so the following use of *Nagayama* is technically unnecessary. However, it does no harm and the examiner leaves this text in place for future use in the event that the claims are again amended: *Yokomizu* does not explicitly

disclose the light shielding portion overlapping at least a channel formation region of the TFT, though they are shown to overlap the switching elements generally, and TFTs inherently have channel regions. *Nagayama* discloses using TFTs with channel regions as the switching elements and having the analogous light shielding portions overlap them [see Fig. 1]. It would have been obvious to one of ordinary skill in the art to do so, motivated by *Nagayama*'s teachings that "using TFTs as switching elements has recently become widely used" [col. 1, lines 28-29], that "the TFT ... comprises a semiconductor layer (a layer in which a channel is formed)" [col. 7, lines 64-65], and that by using a light shield overlapping the active elements "the malfunction of the active elements due to external light can be prevented" [col. 6, lines 1-3].)

Yokomizu also does not disclose that the organic resin film has a thickness of 1 μm or more; the reference appears to be silent on the thickness of the organic resin film. *Kanemoto* discloses [see Fig. 1] analogous overlapping color filters, and discloses that the thickness increase where they overlap is 1-2 μm [col. 3, lines 34-36]. *Yoneya* teaches [col. 17, line 65 – col. 18, line 5] that a function of the organic resin film (overcoat layer) is "to flatten a difference in level due to the color filter and the light-shielding film". It would therefore have been obvious to one of ordinary skill in the art at the time of the invention to make the thickness of the organic resin film large enough to flatten (or at least moderate) a 1-2 μm bump. Doing so requires a thickness of about 1 μm or more, which overlaps the recited range of 1 μm or more; in such cases a *prima facie* case of obviousness exist [see MPEP 2144.05].

Claim 91 is therefore unpatentable.

Regarding the additional limitation of claim 92, that there is a third colored layer in the overlap stack, *Yokomizu* discloses that all three color filters can be stacked to form 21BM [paragraph 0020, for instance], so claim 92 is also unpatentable.

A step (albeit tapered) exists at a portion where the colored layers overlap, so claims 95 and 96 are also unpatentable. The organic resin film is a leveling film, as discussed above with reference to *Yoneya*, so claims 99 and 100 are also unpatentable.

Allowable Subject Matter

5. Claims 101 and 102 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.
6. Claims 21-24, 76, 77, 85-90, 93, 94, 97, and 98 are allowed.
7. The following is a statement of reasons for the indication of allowable subject matter:

The prior art does not disclose the electro-optical device of claim 21, in particular the limitations reciting the following electrode structure: a gate electrode and source wiring, first insulating film formed on them, semiconductor layer formed over the first insulating film, second insulating film covering the semiconductor layer, and gate wiring (connected to gate electrode) and connection wiring (connecting source wiring to semiconductor layer) formed on the second insulating film. Claim 21 is therefore allowed, as are its dependent claims 22-24, 88-90, 93, and 97.

The prior art does not disclose the electro-optical device of claim 76, in particular the limitations reciting the same electrode structure discussed above with respect to claim 21. Claim 76 is therefore allowed, as are its dependent claims 77, 85-87, 94, and 98.

The prior art does not disclose the electro-optical device of claims 101 and 102. Taken together with the limitations recited by their respective independent claims, these claims recite the same electrode discussed above with respect to claims 21 and 76. Claims 101 and 102 would therefore be allowable if rewritten appropriately.

Terminal Disclaimer

8. The three terminal disclaimers filed on 2 July 2008 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of U.S. Patent No. 7,084,019, U.S. Patent No. 6,580,475, and any patent granted on Application No. 11/460,105 have been reviewed and are accepted. The terminal disclaimers have been recorded.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andrew Schechter whose telephone number is (571) 272-2302. The examiner can normally be reached on Monday - Friday, 9:00 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Andrew Schechter/
Primary Examiner, Art Unit 2871
Technology Center 2800
3 August 2008